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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,194	09/26/2003	Toshio Kimura	1035-471	4479

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EXAMINER	
IM, JUNGHWA M	
ART UNIT	**PAPER NUMBER**
2811	
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10/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,194	KIMURA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-10 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita et al. (US 5191405), hereinafter Tomita in view of Gaul (US 5608264)

Regarding claim 1, Fig. 1h of Tomita shows a chip-stack semiconductor device, comprising:

multiple semiconductor chips [1, 6, 15, 23] vertically stacked on top of each other, wherein:

each of the semiconductor chips includes electrode pads [3, 4, 11, 24, 25, 26], and

multiple through electrodes [9, 22, 27] formed in a region of the electrode pads.

Tomita shows most aspects of the instant invention except "at least one type of the through electrodes is a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed." Fig. 5 of Gaul shows stacked semiconductor devices [341-343] wherein at least one type of the through electrodes is a non-contact through electrode [344] that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Gaul into the device of Tomita in order to have at least one type of the through electrodes being a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip to provide air filled connection.

Regarding claim 3, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 1) is contact through electrodes electrically connected to the electrode pad.

Regarding claim 7, Fig. 5 of Gaul that a through electrode is further provided in regions outside of the electrode pad.

Regarding claim 19, Fig. 1h of Tomita shows that the electrode pads are electrically connected with a device region of the semiconductor chip.

Regarding claim 20, Fig. 1h of Tomita shows a chip-stack semiconductor device, comprising:

multiple semiconductor chips [1, 6, 15, 23] vertically stacked on top of each other, and at least first [25 on the chip 23] and second electrode pads [24, 46] provided on at least one of the semiconductor chips wherein:

each of the semiconductor chips includes through electrodes [9, 22, 27] connected to each other in regions inside of electrode pads, each of through electrodes linking a front surface to a back surface of the semiconductor chip; and

each of the semiconductor chips includes multiple through electrodes [3, 4, 11, 24, 25, 26] wherein a plurality of different through electrodes are located inside of the first electrode pad.

Tomita shows most aspects of the instant invention except "at least one type of the through electrodes is a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed." Fig. 5 of Gaul shows stacked semiconductor devices [341-343] wherein at least one type of the through electrodes is a non-contact through electrode [344] that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Gaul into the device of Tomita in order to have at least one type of the through electrodes being a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip to provide air filled connection.

Regarding claim 21, Fig. 1h of Tomita shows a plurality of different through electrodes (the one from the layer 1 and the one from the layer 15) provide in the first electrode pad 925), first and second of these different through electrodes carry different signals.

Regarding claim 22, Fig. 1h of Tomita shows a plurality of different through electrodes (the one from the layer 1 and the one from the layer 15) provide in the first electrode pad [25], first and second of these different through electrodes carry different signals.

Regarding claim 23, Fig. 1h of Tomita show a chip-stack semiconductor device comprising:

multiple semiconductor chips [1, 6, 15, 23] vertically stacked on top of each other, wherein each of the semiconductor chips includes electrode pads [3, 4, 11, 25], and multiple through electrodes formed in a region within the electrode pads, wherein at least two of the through electrodes formed in a region within the same electrode pad [25] wherein the through

electrodes are provided in respective apertures defined in the electrode pads so as to extend through the pads.

Tomita shows most aspects of the instant invention except "at least two of the through electrodes formed in a region within the same electrode pad are not in direct electrical contact with each other." Fig. 5 of Gaul shows stacked semiconductor devices [341-343] wherein at least one type of the through electrodes is a non-contact through electrode [344] that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Gaul into the device of Tomita in order to have at least two of the through electrodes within the same electrode pad not in direct electrical contact with each other for optional aril filled connection.

Claims 2, 4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita in view of Gaul as applied to claims 1 and 20 above further in view of Tsunashima (US 6087719).

Regarding claim 2, the combination of Tomita/Gaul shows most aspects of the instant invention except "at least one semiconductor chip the electrode pads are provided along a periphery of the semiconductor chip so as to surround a device region." Fig. 3B of Tsunashima shows a stacked semiconductor device wherein for at least one semiconductor chip the electrode pads are provided along a periphery of the semiconductor chip so as to surround a device region.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tsunashima into the device of Tomita/Gaul in order to have the electrode pads along a periphery of the semiconductor chip for electrical connection to an outer device.

Regarding claim 4, Fig. 1h of Tomita shows that at least one type of the through electrodes (the one connected from the layer 1) is contact through electrodes electrically connected to the electrode pad.

Regarding claim 8, Fig. 5 of Gaul shows that a through electrode is further provided in regions outside of the electrode pad.

Regarding claims 9-10, Fig. 1h of Tomita shows most aspects of the instant invention except "the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other." Fig. 1 of Tsunashima shows that the through electrodes in the semiconductor chips are connected to each other via bumps [9] so that the semiconductor chips are vertically stacked on top of each other.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tsunashima into the device of Tomita in order to have the through electrodes in the semiconductor chips connected to each other via bumps to secure the connection

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junghwa M. Im
Examiner
Art Unit 2811

jmi
10/9/2007